| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| E | Removed vendor CAGE numbers 18324, 27014, and 34335. Added devices 21 and 22. Updated document format, editorial changes throughout. | 96-06-13 | M. A. Frye |
| F | Updated boilerplate. Removed vendor CAGE number 50364 from drawing. - glg | 01-01-11 | Raymond Monnin |
| G | Boilerplate update, part of 5 year review. ksr | 06-08-18 | Raymond Monnin |
| H | Updated boilerplate to current MIL-PRF-38535 requirements. - llb | 15-03-19 | Charles Saffle |

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | H | H | H | H | | | | | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | | | | | | | | | | | | | | | | |

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV STATUS | REV | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |

PMIC N/A

PREPARED BY
James Jamison

**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**http://www.landandmaritime.dla.mil**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles Reusing

APPROVED BY
Michael. A. Frye

DRAWING APPROVAL DATE
86-06-20

MICROCIRCUIT, MEMORY, BIPOLAR, PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

REVISION LEVEL
H

| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-85155** |

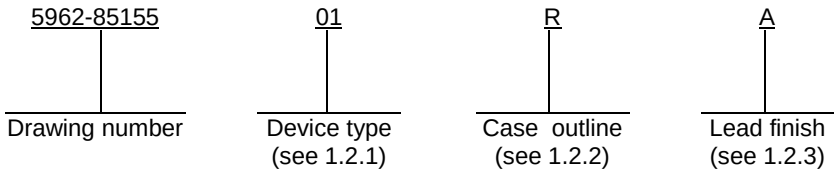
SHEET 1 OF 18

DSCC FORM 2233
APR 97

5962-E183-15

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:




1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

| Device type | Generic number | Circuit |
|---|---|---|
| 01 | PAL16L8-20 | 16-input 8-output AND-OR invert gate array |
| 02 | PAL16R8-20 | 16-input 8-output registered AND-OR gate array |
| 03 | PAL16R6-20 | 16-input 6-output registered AND-OR gate array |
| 04 | PAL16R4-20 | 16-input 4-output registered AND-OR gate array |
| 05 | PAL16L8-30 | 16-input 8-output AND-OR invert gate array |
| 06 | PAL16R8-30 | 16-input 8-output registered AND-OR gate array |
| 07 | PAL16R6-30 | 16-input 6-output registered AND-OR gate array |
| 08 | PAL16R4-30 | 16-input 4-output registered AND-OR gate array |
| 09 | PAL16L8-15 | 16-input 8-output AND-OR invert gate array |
| 10 | PAL16R8-15 | 16-input 8-output registered AND-OR gate array |
| 11 | PAL16R6-15 | 16-input 6-output registered AND-OR gate array |
| 12 | PAL16R4-15 | 16-input 4-output registered AND-OR gate array |
| 13 | PAL16L8A-12 | 16-input 8-output AND-OR invert gate array |
| 14 | PAL16R8A-12 | 16-input 8-output registered AND-OR gate array |
| 15 | PAL16R6-12 | 16-input 6-output registered AND-OR gate array |
| 16 | PAL16R4-12 | 16-input 4-output registered AND-OR gate array |
| 17 | PAL16L8-10 | 16-input 8-output AND-OR invert gate array |
| 18 | PAL16R8-10 | 16-input 8-output registered AND-OR gate array |
| 19 | PAL16R6-10 | 16-input 6-output registered AND-OR gate array |
| 20 | PAL16R4-10 | 16-input 4-output registered AND-OR gate array |
| 21 | PAL16R8-7 | 16-input 8-output registered AND-OR gate array |
| 22 | PAL16R4-7 | 16-input 4-output registered AND-OR gate array |

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| R | GDIP1-T20 or CDIP1-T20 | 20-lead | dual-in-line package |
| S | CDFP5-F20 1/ | 20-lead | flat package |
| 2 | CQCC1-N20 | 20-terminal | square chip carrier package |

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1/ Inactive for new design. Acceptable only for use in equipment designed or redesigned on or before 29 November 1986.

1.3 Absolute maximum ratings.

| | |
|---|---|
| Supply voltage range 2/ | -0.5 V dc to +7.0 V dc |
| Input voltage range 2/ 3/ | -0.5 V dc to +5.5 V dc |
| Storage temperature range | -65°C to +150°C |
| Lead temperature (soldering, 10 seconds) | +260°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$) 4/ | See MIL-STD-1835 |
| Applied voltage to disabled output range 2/ 3/ | -0.5 V dc to +5.5 V dc |
| Maximum power dissipation ($P_D$): 5/ | |
| Device types 01-04 | 1.1 W |
| Device types 05-08 | 0.6 W |
| Device types 09-22 | 1.2 W |
| Maximum junction temperature ($T_J$) | +175°C |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | 4.5 V dc minimum to 5.5 V dc maximum |
| Minimum high level input voltage ($V_{IH}$) | 2.0 V dc |
| Maximum low level input voltage ($V_{IL}$) | 0.8 V dc |
| Maximum high level output current ($I_{OH}$) | -2.0 mA dc |
| Maximum low level output current ($I_{OL}$) | 12.0 mA dc |
| Case operating temperature range ($T_C$) | -55°C to +125°C |

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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2/ These ratings apply except for programming pins during a programming cycle.
3/ To ensure high speed operation, input logic levels must be maintained within these conditions.
4/ Heat sinking is recommended to reduce the junction temperature.
5/ Must withstand the added $P_D$ due to short-circuit test; e.g., $I_{OS}$.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.3.1c), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of fuses shall be programmed) or to any altered item drawing pattern which programs at least 25 percent of the total number of fuses programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.6.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.6.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

3.7 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.7.1 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7.2 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>$-55^oC \le T_C \le +125^oC$<br>unless otherwise specified | | Group A Subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Input clamp voltage | $V_{IC}$ | $V_{CC}$ = 4.5 V, $I_I$ = -18 mA | | 1, 2, 3 | All | | -1.5 | V |
| High Level output voltage | $V_{OH}$ | $V_{CC}$ = 4.5 V, $V_{IL}$ 4.5 V, $V_{IH}$ 2.0 V, $I_{OH}$ = -2 mA | | 1, 2, 3 | 01,02, 04-20 | 2.4 | | V |
| | | | | | 03,21, 22 | 2.3 | | |
| Low level output voltage | $V_{OL}$ | $V_{CC}$ = 4.5 V, $V_{IL}$ 4.5 V, $V_{IH}$ 2.0 V, $I_{OL}$ = 12 mA | | 1, 2, 3 | All | | 0.5 | V |
| High level input voltage | $V_{IH}$ | | | 1, 2, 3 | All | 2 | | V |
| Low level input voltage | $V_{IL}$ | | | 1, 2, 3 | All | | 0.8 | V |
| High level input current | $I_{IH}$ | $V_{CC}$ = 5.5 V, $V_I$ = 2.4 V | Pins CLK and $\overline{OE}$ | 1, 2, 3 | 02,03,04, 06,07,08, 10,11,12, 14,15,16, 18,19,20 | | 50 | µA |
| | | | All others except I/O | | All | | 25 | |
| | | | All I/O ports | | 01,03, 04,05, 07,08, 09,11, 12,13, 15,16, 17,19, 20,21, 22 | | 100 | |
| Low level input current | $I_{IL}$ | $V_{CC}$ = 5.5 V, $V_{IL}$ = 0.4 V | | 1, 2, 3 | All | | -0.25 | mA |
| Input current | $I_I$ | $V_{CC}$ = 5.5 V, $V_I$ = 5.5 V | | 1, 2, 3 | All | | 1 | mA |
| Output current short circuit 1/ | $I_{OS}$ | $V_{CC}$ = 5.5 V, $V_O$ = 0.5 V | | 1, 2, 3 | 01-16 | -30 | -250 | mA |
| | | | | | 17-22 | -30 | -130 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>$-55^{o}C \le T_C \le +125^{o}C$<br>unless otherwise specified | Group A Subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Off-state output current | $I_{OZL}$ | $V_{CC}$ = 5.5 V, $V_O$ = 0.4 V; Outputs | 1, 2, 3 | All | | -100 | µA |
| | | $V_{CC}$ = 5.5 V, $V_O$ = 0.4 V; I/O ports | | | | -250 | |
| Off-state output current | $I_{OZH}$ | $V_{CC}$ = 5.5 V, $V_O$ = 2.4 V | 1, 2, 3 | All | | 100 | µA |
| Supply current | $I_{CC}$ | $V_{CC}$ = 5.5 V, $V_I$ = 0 V<br>Outputs open | 1, 2, 3 | 01-04 | | 190 | mA |
| | | | | 05-08 | | 105 | |
| | | | | 09-20 | | 220 | |
| | | | | 21,22 | | 210 | |
| Functional tests | | See notes for Table II | All | 7, 8 | | | |
| Propagation delay data input to output | $t_{PLH1}$ | See figure 3 | 9, 10, 11 | 01,03,04 | | 20 | ns |
| | | | | 05,07,08 | | 30 | |
| | | | | 09,11,12 | | 15 | |
| | | | | 13,15,16 | | 12 | |
| | | | | 17,19,20 | | 10 | |
| | | | | 21,22 | | 7 | |
| Propagation delay data input to output | $t_{PHL1}$ | | | 01,03,04 | | 20 | |
| | | | | 05,07,08 | | 30 | |
| | | | | 09,11,12 | | 15 | |
| | | | | 13,15,16 | | 12 | |
| | | | | 17,19,20 | | 10 | |
| | | | | 21,22 | | 7 | |
| Propagation delay clock/up to output | $t_{PHL2}$ | | | 02 - 04 | | 15 | |
| | | | | 06 - 08 | | 20 | |
| | | | | 10 - 12, 14,16 | | 12 | |
| | | | | 18, 20 | | 10 | |
| | | | | 21, 22 | | 7 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>$-55^{o}C \le T_C \le +125^{o}C$<br>unless otherwise specified | Group A Subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Propagation delay clock/up to output | $t_{PLH2}$ | See figure 3 | 9, 10, 11 | 02 - 04 | | 15 | ns |
| | | | | 06 - 08 | | 20 | |
| | | | | 10 - 12, 14,16 | | 12 | |
| | | | | 18 - 20 | | 10 | |
| | | | | 21, 22 | | 7 | |
| Propagation delay output high impedance to output high | $t_{PZH1}$ | | | 01,03,04 | | 25 | |
| | | | | 05,07,08 | | 30 | |
| | | | | 09,11,12 | | 17 | |
| | | | | 13,15,16 | | 14 | |
| | | | | 17,19,20 | | 12 | |
| | | | | 21,22 | | 9 | |
| Propagation delay output high impedance to output low | $t_{PZL1}$ | | | 01,03,04 | | 25 | |
| | | | | 05,07,08 | | 30 | |
| | | | | 09,11,12 | | 17 | |
| | | | | 13,15,16 | | 14 | |
| | | | | 17,19,20 | | 12 | |
| | | | | 21,22 | | 9 | |
| Propagation delay output high to output high impedance 2/ | $t_{PHZ1}$ | | | 01,03,04 | | 20 | |
| | | | | 05,07,08 | | 30 | |
| | | | | 09,11,12 | | 15 | |
| | | | | 13,15,16 | | 12 | |
| | | | | 17,19, 20,21, 22 | | 10 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>$-55^{o}C \le T_C \le +125^{o}C$<br>unless otherwise specified | Group A Subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Propagation delay output low to output high impedance 2/ | $t_{PLZ1}$ | See figure 4 | 9, 10, 11 | 01,03,04 | | 20 | ns |
| | | | | 05,07,08 | | 30 | |
| | | | | 09,11,12 | | 15 | |
| | | | | 13,15,16 | | 12 | |
| | | | | 17,19, 20,21,22 | | 10 | |
| Propagation delay high impedance to output high ($\overline{OE}$ to output enable) 3/ | $t_{PZH2}$ | | | 01,03,04 | | 20 | |
| | | | | 05,07,08 | | 30 | |
| | | | | 09,11,12 | | 15 | |
| | | | | 13,15,16 | | 12 | |
| | | | | 17,19,20 | | 10 | |
| | | | | 21,22 | | 8 | |
| Propagation delay high impedance to output low ($\overline{OE}$ to output enable) 3/ | $t_{PZL2}$ | | | 02,03,04 | | 20 | |
| | | | | 06,07,08 | | 25 | |
| | | | | 10,11,12, 14 - 16 | | 12 | |
| | | | | 18 - 20 | | 10 | |
| | | | | 21,22 | | 8 | |
| Propagation delay output high to high impedance ($\overline{OE}$ to output disable) 2/ 3/ | $t_{PHZ2}$ | | | 02,03,04 | | 20 | |
| | | | | 06,07,08 | | 25 | |
| | | | | 10,11,12, 14 - 16 | | 12 | |
| | | | | 18 - 20, 21,22 | | 10 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>$-55^{o}C \le T_C \le +125^{o}C$<br>unless otherwise specified | Group A Subgroups | Device Type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Propagation delay output low to high impedance<br>( $\overline{OE}$ to output disable)<br>2/ 3/ | $t_{PLZ2}$ | See figure 3 | 9, 10, 11 | 02,03,04 | | 20 | ns |
| | | | | 06,07,08 | | 25 | |
| | | | | 10,11,12, 14 - 16 | | 12 | |
| | | | | 18 - 20, 21,22 | | 10 | |
| Clock pulse width, high<br>4/ | $t_{PCLH}$ | | | 02,03,04 | 12 | | |
| | | | | 06,07,08 | 20 | | |
| | | | | 10,11,12, 14 - 16 | 9 | | |
| | | | | 18 - 20 | 8 | | |
| | | | | 21,22 | 5 | | |
| Clock pulse width, low<br>4/ | $t_{PCLL}$ | | | 02 - 04, 10 - 12 | 12 | | |
| | | | | 06,07,08 | 20 | | |
| | | | | 14 - 16 | 9 | | |
| | | | | 18 - 20 | 8 | | |
| | | | | 21,22 | 5 | | |

See footnotes at end of table.

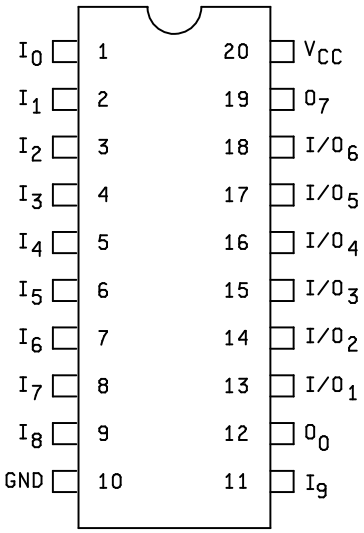
TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>$-55^{o}C \le T_C \le +125^{o}C$<br>unless otherwise specified | Group A Subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Hold time | $t_H$ | See figure 4 | 9, 10, 11 | 02,03,04, 06,07,08, 10,11,12, 14,15,16, 18,20,21, 22 | 0 | | ns |
| Setup time | $t_{SU}$ | | | 02,03,04 | 20 | | |
| | | | | 06,07,08 | 30 | | |
| | | | | 10,11,12 | 15 | | |
| | | | | 14 - 16, 18 - 20 | 11 | | |
| | | | | 21,22 | 7 | | |
| Maximum clock frequency data path register | $f_{MAX}$ | | | 02,03,04 | 41.6 | | MHz |
| | | | | 06,07,08 | 25.0 | | |
| | | | | 10,11,12 | 50.0 | | |
| | | | | 14 - 16 | 56.0 | | |
| | | | | 18 - 20 | 62.5 | | |
| | | | | 21,22 | 100 | | |

1/ The output conditions may be chosen to produce a current that closely approximates one-half of the true short-circuit output current, $I_{OS}$.
2/ Testing shall be performed using $C_L = 5$ pF.
3/ Test applies only to register outputs.
4/ The total clock period of CLK high and CLK low must not exceed clock frequency, $f_{clock}$. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

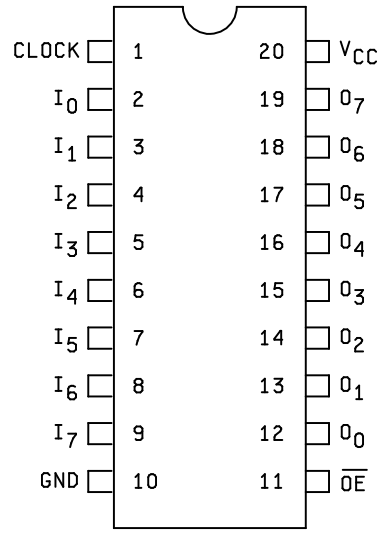
DEVICE TYPES 01,05,09,13, AND 17

CASE R AND S



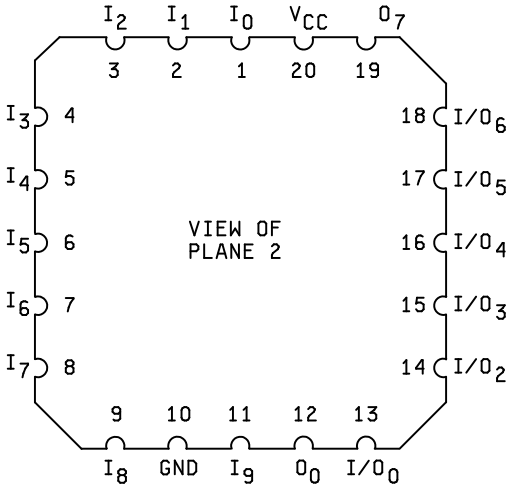

DEVICE TYPES 02,06,10,14,18, AND 21

CASE R AND S




DEVICE TYPES 01,05,09,13, AND 17

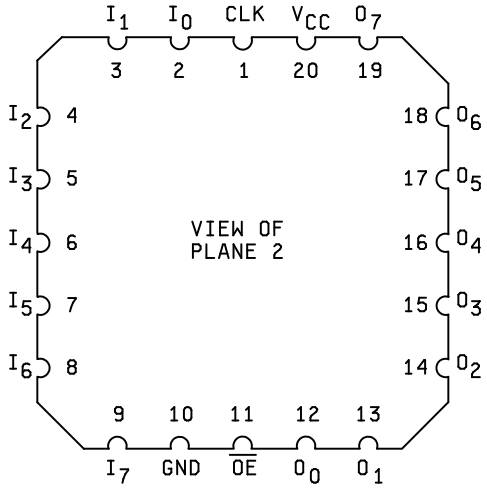
CASE 2




Option A with active terminals on plane 1.

DEVICE TYPES 02,06,10,14,18, AND 21

CASE 2

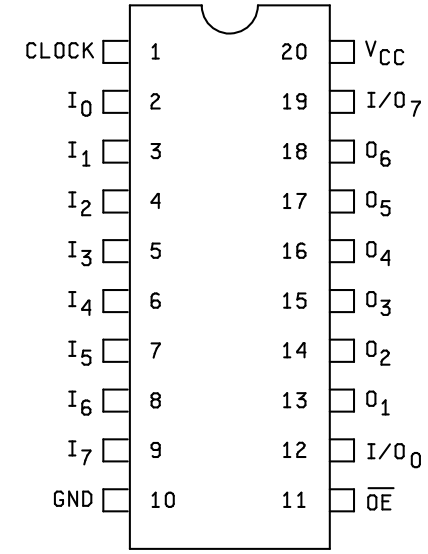



Option A with active terminals on plane 1.

FIGURE 1. Terminal connections.

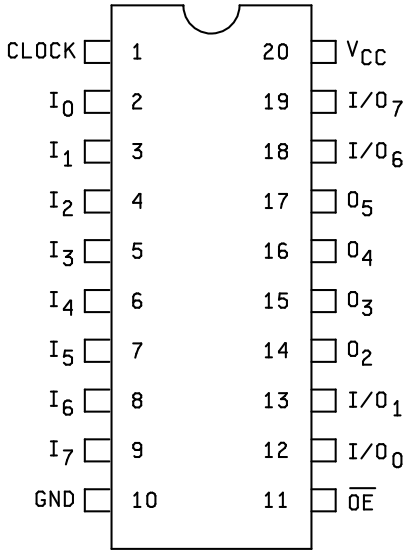
DEVICE TYPES 03,07,11,15, AND 19

CASE R AND S



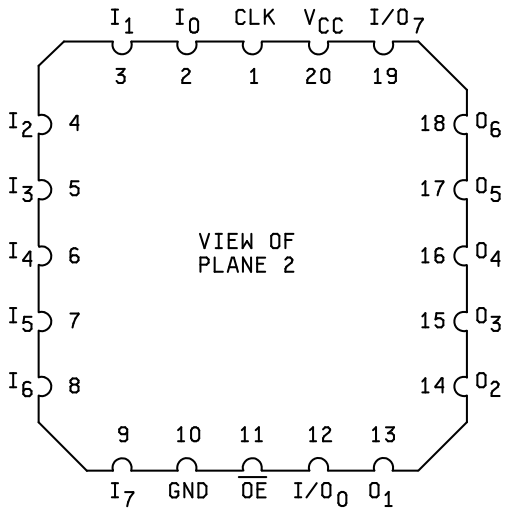

DEVICE TYPES 04,08,12,16,20, AND 22

CASE R AND S




DEVICE TYPES 03,07,11,15, AND 19

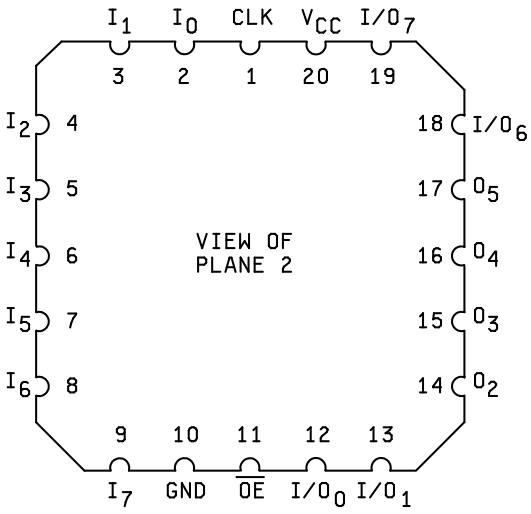
CASE 2




Option A with active terminals on plane 1.

DEVICE TYPES 04,08,12,16,20, AND 22

CASE 2




Option A with active terminals on plane 1.

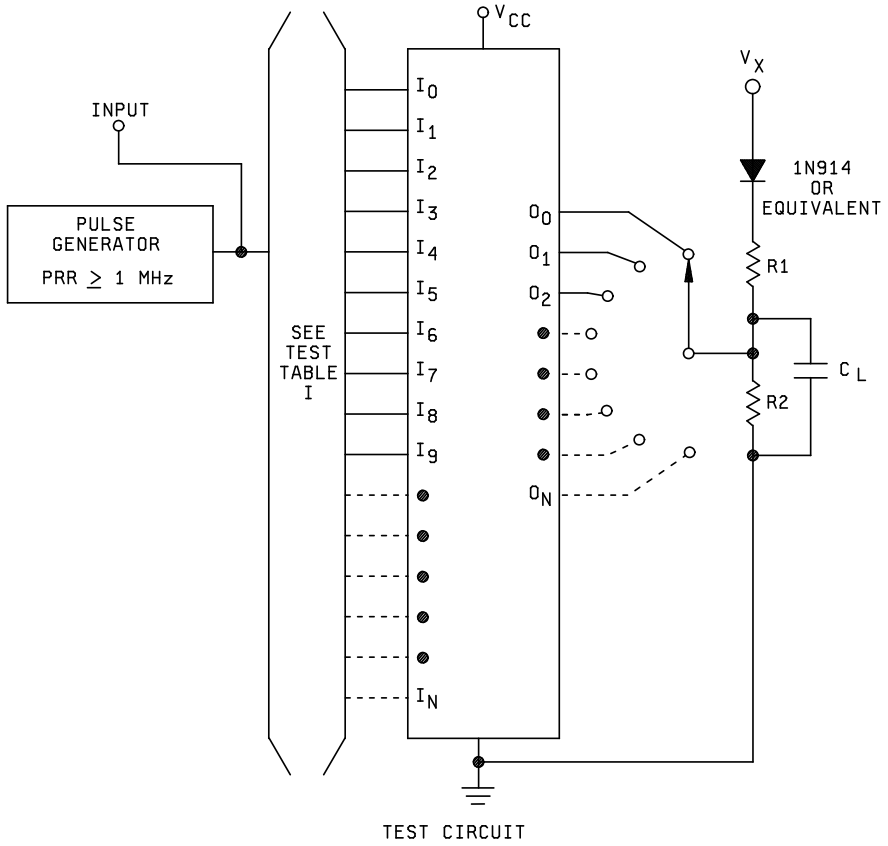
FIGURE 1. Terminal connections - Continued.

Device types 01 through 22

| Truth table | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | | | | | | | | | | | Output level | | | | | | | | |
| CK | OE | $I_9$ | $I_8$ | $I_7$ | $I_6$ | $I_5$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | $O_7$ | $O_6$ | $O_5$ | $O_4$ | $O_3$ | $O_2$ | $O_1$ | $O_0$ | Device |
| | | X | X | X | X | X | X | X | X | X | X | Z | Z | Z | Z | Z | Z | Z | Z | 01, 05, 09, 13, 17 |
| CK | L | | | X | X | X | X | X | X | X | X | H | H | H | H | H | H | H | H | 02, 06, 10, 14, 18, 21 |
| CK | L | | | X | X | X | X | X | X | X | X | Z | H | H | H | H | H | H | Z | 03, 07, 11, 15, 19 |
| CK | L | | | X | X | X | X | X | X | X | X | Z | Z | H | H | H | H | Z | Z | 04, 08,12, 16, 20, 22 |

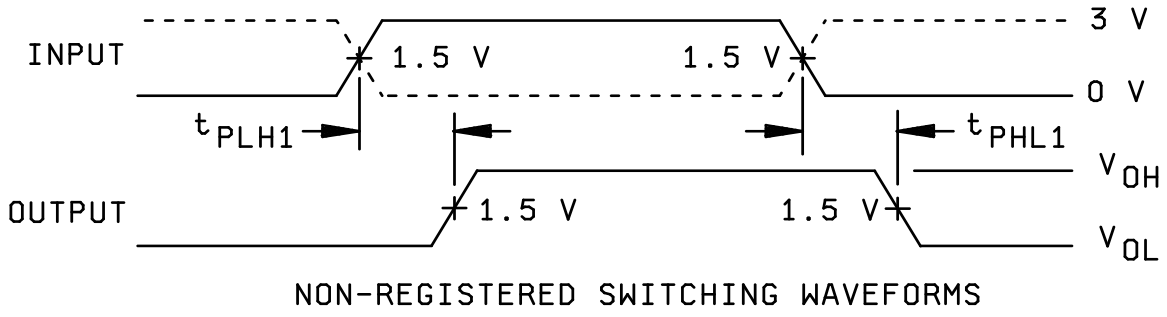
NOTES:
1. Z = three-state.
2. Clock (pin 1): Low to high transition required to obtain valid data after last address transition.
3. Enable (pin 11): Must be low to enable output.

FIGURE 2. Truth table (unprogrammed).



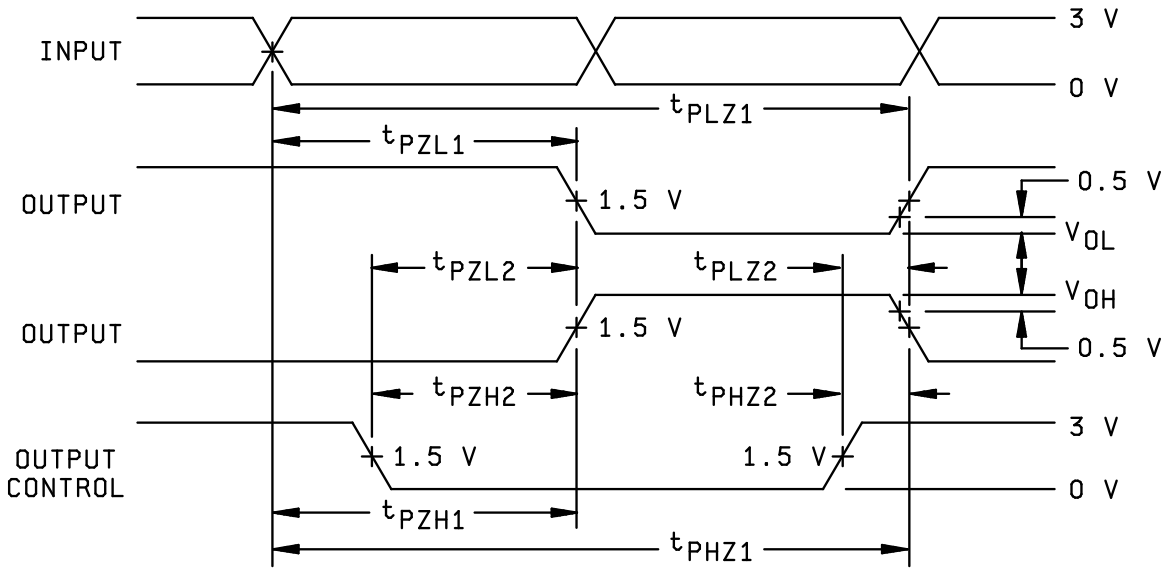

TEST CIRCUIT

NOTES:
1. $C_L$ = 50 pF minimum, including jig and probe capacitance; R1 = 365Ω ±2%; R2 = 715Ω ± 2%.
2. The tests shall check all inputs, gates, and outputs that have been programmed. The test shall be performed $V_{CC}$ = 4.5 V and 5.5 V.
3. $V_X$ = 5.7 V for $t_{PLH}$, $t_{PHL}$, $t_{PZL}$, and $t_{PLZ}$ tests and 0 V for $t_{PHZ}$, $t_{PZH}$ and $f_{max}$ tests.

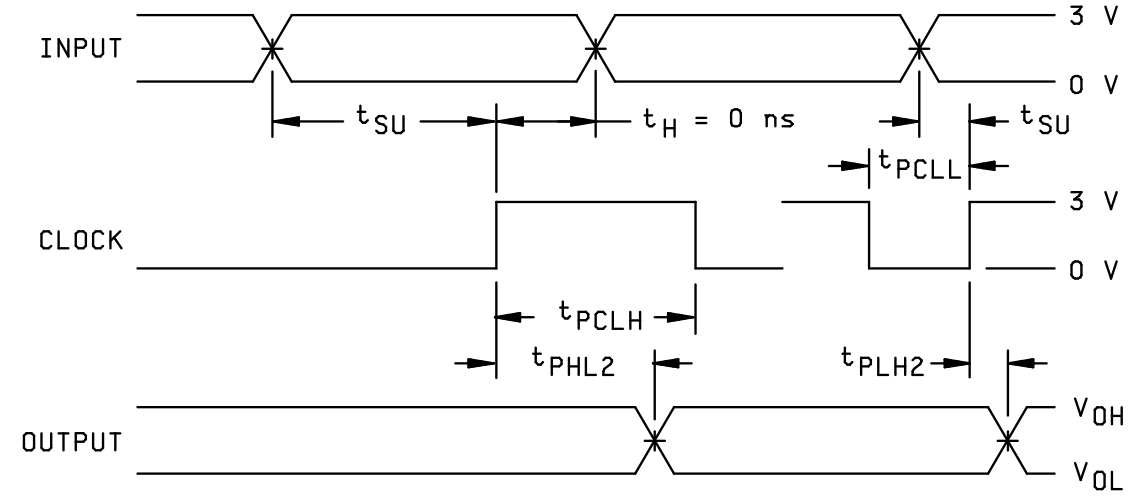



NON-REGISTERED SWITCHING WAVEFORMS

FIGURE 3. Test circuit and switching waveforms.




INPUT AND OUTPUT CONTROL SWITCHING WAVEFORM




REGISTERED SWITCHING WAVEFORM

FIGURE 3. Test circuit and switching waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of the two following techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in method 5005 of MIL-STD-883.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail, the lot shall be rejected. At the manufacturers option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements. 1/, 2/, 3/, 4/

| MIL-STD-883 test requirements | Subgroups (per method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | 1 |
| Final electrical test parameters (method 5004) for unprogrammed devices | 1**, 2, 3, 7**, 8 |
| Final electrical test parameters (method 5004) for programmed devices | 1**, 2, 3, 7**, 8, 9 |
| Group A test requirements (method 5005) | 1, 2, 3, 7, 8, 9, 10***, 11*** |
| Groups C and D end-point electrical parameters (method 5005) | 1, 2, 3, 7, 8 |

1/ * Indicates any or all subgroups may be combined when using high-speed testers.
2/ Subgroups 7 and 8 functional tests shall verify the truth table of figure 2, for unprogrammed or that the altered item drawing pattern exists for programmed devices.
3/ ** Indicates PDA applies to subgroups 1 and 7.
4/ *** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-03-19

Approved sources of supply for SMD 5962-85155 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-85155012A | 01295<br>3/ | TIBPAL16L8-20MFKB<br>PAL16L8BML/883B |
| 5962-8515501RA | 01295<br>3/<br>3/ | TIBPAL16L8-20MJB<br>PAL16L8J/883<br>PAL16L8BMJ/883B |
| 5962-8515501SA | 01295<br>3/ | TIBPAL16L8-20MWB<br>PAL16L8BMW/883B |
| 5962-85155022A | 01295<br>3/ | TIBPAL16R8-20MFKB<br>PAL16R8BML/883B |
| 5962-8515502RA | 01295<br>3/<br>3/ | TIBPAL16R8-20MJB<br>PAL16R8J/883<br>PAL16R8BMJ/883B |
| 5962-8515502SA | 01295<br>3/ | TIBPAL16R8-20MWB<br>PAL16R8BMW/883B |
| 5962-85155032A | 01295<br>3/ | TIBPAL16R6-20MFKB<br>PAL16R6BML/883B |
| 5962-8515503RA | 01295<br>3/<br>3/ | TIBPAL16R6-20MJB<br>PAL16R6J/883<br>PAL16R6BMJ/883B |
| 5962-8515503SA | 01295<br>3/ | TIBPAL16R6-20MWB<br>PAL16R6BMW/883B |
| 5962-85155042A | 01295<br>3/ | TIBPAL16R4-20MFKB<br>PAL16R4BML/883B |
| 5962-8515504RA | 01295<br>3/<br>3/ | TIBPAL16R4-20MJB<br>PAL16R4J/883<br>PAL16R4BMJ/883B |
| 5962-8515504SA | 01295<br>3/ | TIBPAL16R4-20MWB<br>PAL16R4BMW/883B |
| 5962-85155052A | 01295<br>3/ | TIBPAL16L8-30MFKB<br>PAL16L8B-2ML/883B |

See footnotes at end of table.

| Standard microcircuit 1/ drawing PIN | Vendor CAGE number | Vendor similar 2/ PIN |
|---|---|---|
| 5962-8515505RA | 01295<br>3/<br>3/ | TIBPAL16L8-30MJB<br>PAL16L8B2J/883<br>PAL16L8B-2MJ/883B |
| 5962-8515505SA | 01295<br>3/ | TIBPAL16L8-30MWB<br>PAL16L8B-2MW/883B |
| 5962-85155062A | 01295<br>3/ | TIBPAL16R8-30MFKB<br>PAL16R8B-2ML/883B |
| 5962-8515506RA | 01295<br>3/<br>3/ | TIBPAL16R8-30MJB<br>PAL16R8B2J/883<br>PAL16R8B-2MJ/883B |
| 5962-8515506SA | 01295<br>3/ | TIBPAL16R8-30MWB<br>PAL16R8B-2MW/883B |
| 5962-85155072A | 01295<br>3/ | TIBPAL16R6-30MFKB<br>PAL16R6B-2ML/883B |
| 5962-8515507RA | 01295<br>3/<br>3/ | TIBPAL16R6-30MJB<br>PAL16R6B2J/883<br>PAL16R6B-2MJ/883B |
| 5962-8515507SA | 01295<br>3/ | TIBPAL16R6-30MWB<br>PAL16R6B-2MW/883B |
| 5962-85155082A | 01295<br>3/ | TIBPAL16R4-30MFKB<br>PAL16R4B-2ML/883B |
| 5962-8515508RA | 01295<br>3/<br>3/ | TIBPAL16R4-30MJB<br>PAL16R4B2J/883<br>PAL16R4B-2MJ/883B |
| 5962-8515508SA | 01295<br>3/ | TIBPAL16R4-30MWB<br>PAL16R4B-2MW/883B |
| 5962-85155092A | 01295<br>3/<br>3/ | TIBPAL16L8-15MFKB<br>PLUS16L8/B2A<br>PAL16L8DML/883B3B |
| 5962-8515509RA | 01295<br>3/<br>3/ | TIBPAL16L8-15MJB<br>PLUS16L8/BRA<br>PAL16L8DMJ/883B |
| 5962-8515509SA | 01295<br>3/<br>3/ | TIBPAL16L8-15MWB<br>PLUS16L8/BSA<br>PAL16L8DMW/883B |
| 5962-85155102A | 3/<br>3/<br>3/ | TIBPAL16R8-15MFKB<br>PLUS16R8/B2A<br>PAL16R8DML/883B3B |

See footnotes at end of table.

| Standard microcircuit 1/ drawing PIN | Vendor CAGE number | Vendor similar 2/ PIN |
|---|---|---|
| 5962-8515510RA | 3/<br>3/<br>3/ | TIBPAL16R8-15MJB<br>PLUS16R8/BRA<br>PAL16R8DMJ/883B |
| 5962-8515510SA | 3/<br>3/<br>3/ | TIBPAL16R8-15MWB<br>PLUS16R8/BSA<br>PAL16R8DMW/883B |
| 5962-85155112A | 3/<br>3/ | TIBPAL16R6-15MFKB<br>PAL16R6DML/883B |
| 5962-8515511RA | 3/<br>3/ | TIBPAL16R6-15MJB<br>PAL16R6DMJ/883B |
| 5962-8515511SA | 3/<br>3/ | TIBPAL16R6-15MWB<br>PAL16R6DMW/883B |
| 5962-85155122A | 01295<br>3/ | TIBPAL16R4-15MFKB<br>PAL16R4DML/883B |
| 5962-8515512RA | 01295<br>3/ | TIBPAL16R4-15MJB<br>PAL16R4DMJ/883B |
| 5962-8515512SA | 01295<br>3/ | TIBPAL16R4-15MWB<br>PAL16R4DMW/883B |
| 5962-85155132A | 01295<br>3/ | TIBPAL16L8-12MFKB<br>PLUS16L8A/B2A |
| 5962-8515513RA | 01295<br>3/<br>3/ | TIBPAL16L8-12MJB<br>PLUS16L8A/BRA<br>PAL16L8-12/BRA |
| 5962-8515513SA | 01295<br>3/ | TIBPAL16L8-12MWB<br>PLUS16L8A/BSA |
| 5962-85155142A | 3/<br>3/ | TIBPAL16R8-12MFKB<br>PLUS16R8A/B2A |
| 5962-8515514RA | 3/<br>3/<br>3/ | TIBPAL16R8-12MJB<br>PLUS16R8A/BSA<br>PAL16R8-12/BRA |
| 5962-8515514SA | 3/<br>3/ | TIBPAL16R8-12MWB<br>PLUS16R8A/BSA |
| 5962-85155152A | 01295 | TIBPAL16R6-12MFKB |
| 5962-8515515RA | 01295<br>3/ | TIBPAL16R6-12MJB<br>PAL16R6-12/BRA |

See footnotes at end of table.

| Standard microcircuit 1/ drawing PIN | Vendor CAGE number | Vendor similar 2/ PIN |
|---|---|---|
| 5962-8515515SA | 01295 | TIBPAL16R6-12MWB |
| 5962-85155162A | 01295 | TIBPAL16R4-12MFKB |
| 5962-8515516RA | 01295<br>3/ | TIBPAL16R4-12MJB<br>PAL16R4-12/BRA |
| 5962-8515516SA | 01295 | TIBPAL16R4-12MWB |
| 5962-85155172A | 3/ | TIBPAL16L8-10MFKB |
| 5962-8515517RA | 3/<br>3/ | TIBPAL16L8-10MJB<br>PAL16L8-10/BRA |
| 5962-8515517SA | 3/ | TIBPAL16L8-10MWB |
| 5962-85155182A | 01295 | TIBPAL16R8-10MFKB |
| 5962-8515518RA | 01295<br>3/ | TIBPAL16R8-10MJB<br>PAL16R8-10/BRA |
| 5962-8515518SA | 01295 | TIBPAL16R8-10MWB |
| 5962-85155192A | 3/ | TIBPAL16R6-10MFKB |
| 5962-8515519RA | 01295<br>3/ | TIBPAL16R6-10MJB<br>PAL16R6-10/BRA |
| 5962-8515519SA | 3/ | TIBPAL16R6-10MWB |
| 5962-85155202A | 3/ | TIBPAL16R4-10MFKB |
| 5962-8515520RA | 3/<br>3/ | TIBPAL16R4-10MJB<br>PAL16R4-10/BRA |
| 5962-8515520SA | 3/ | TIBPAL16R4-10MWB |
| 5962-85155212A | 01295 | TIBPAL16R8-7MFKB |
| 5962-8515521RA | 01295 | TIBPAL16R8-7MJB |

See footnotes at end of table.

| Standard microcircuit 1/ drawing PIN | Vendor CAGE number | Vendor similar 2/ PIN |
|---|---|---|
| 5962-8515521SA | 01295 | TIBPAL16R8-7MWB |
| 5962-85155222A | 3/ | TIBPAL16R4-7MFKB |
| 5962-8515522RA | 3/ | TIBPAL16R4-7MJB |
| 5962-8515522SA | 3/ | TIBPAL16R4-7MWB |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest Ln.<br>PO Box 660199<br>Dallas, TX 75243<br>Point of contact: U.S. Highway 75 South<br>P.O. Box 84, M/S 853<br>Sherman, TX 75090-9493 |